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EXAMINER	
URICK, MATTHEW T	

ART UNIT	PAPER NUMBER
2113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,887	ACKARET ET AL.	
	Examiner	Art Unit	
	Matt Urick	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7* is/are allowed.

6)☒ Claim(s) *8-10 and 16-19* is/are rejected.

7)☒ Claim(s) *11-15,20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Non-Final Official Action

Status of the Claims

Claims 1-7 are allowable

Claims 8-10, 16-19 are rejected under 35 USC 103

Claim 9 is objected to under 37 CFR 1.75(c)

Claims 11-15, 20 and 21 are objected to while containing allowable matter

Claim Objections

Claim 9 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The limitations of claim 9 - "to track the number of consecutive errors associated with any particular system memory address" and "to increase the frequency of said polling if the number of consecutive errors associated with a particular memory address equals a first threshold" – are already claimed identically in claim 8.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig (United States Patent No. 6,505,305) in view of Kwiat (United States Patent No. 6,363,496).

As per claim 16, Olarig discloses:

A system management device suitable for use in a data processing system comprising a processor coupled to a system memory, wherein the system management device is configured to

retrieve system memory error information including any corresponding system memory address information from the processor following assertion of the signal (column 10 line 55 – column 11 lines 3 "the address is saved in the tag storage area");

and

track the number of system memory errors corresponding to any particular system memory address (column 10 line 65 – column 11 line 3; column 11 lines 12-16: errors relating to each address are recorded in storage area 328 and the total number of errors for each location is compared to a threshold); and

issue an alert if the number of system memory errors corresponding to a particular system memory address equals a specified maximum value (column 11 lines 12-16: number of errors compared to a threshold, lines 37-43: an indicator is asserted if the threshold is exceeded).

Olarig does not disclose:

implement a watchdog timer and to assert a signal periodically to interrupt the processor;

Olarig's detects faults by remaining in a constant loop until faults are detected (Olarig column 10 lines 59-67: constant loop at step 400). This requires the memory controller 300 to constantly query the ECC logic component, increasing the activity in the memory controller, and decreasing its ability to perform other tasks, such as controlling data transfer between the processor and the memory array (column 7 lines 32-36: memory controller controls all traffic between processor and memory array). Kwiat discloses a system involving an adjustable watchdog timer which periodically queries a group of components to determine if they are working correctly (column 7 lines 52-54). Kwiat discloses that this periodic polling effectively decreases traffic in the system and increases throughput, without creating excessively long delays in fault detection (column 2 lines 33-40, lines 55-62). Olarig wishes to increase the performance of the computer system and minimize failover time (column 2 lines 33-40, 56-62). Using Kwiat's adjustable watchdog timer would decrease the excess load on the memory controller while still maintaining an effective means for fault detection in the memory array. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the adjustable watchdog timer of Kwiat into the memory failover system of Olarig, decreasing the load on the memory controller and maintaining effective fault detection.

As per claim 17, Olarig discloses:

The management device of claim 16, further configured to assert the signal by asserting a general purpose I/O pin (column 6 lines 15-29: the system includes an I/O controller capable of connecting various input and output devices: column 5 lines 3-6: an LED or a message on a display connected to the I/O controller may be be used to indicate the alert to the user).

As per claim 18, Olarig discloses:

The management device of claim 16, further configured to track the number of consecutive system memory errors corresponding to any particular system memory address (column 11 lines 12-16).

As per claim 19, Olarig fails to disclose:

The management device of claim 16, further configured to increase the frequency of interrupting the processor if the number of errors associated with any particular memory address equals a first threshold.

Olarig's detects faults by remaining in a constant loop until faults are detected (Olarig column 10 lines 59-67: constant loop at step 400). This requires the memory controller 300 to constantly query the ECC logic component, increasing the activity in the memory controller, and decreasing its ability to perform other tasks, such as controlling data transfer between the processor and the memory array (column 7 lines 32-36: memory controller controls all traffic between processor and memory array).

Kwiat discloses a system involving an adjustable watchdog timer which periodically queries a group of components to determine if they are working correctly (column 7 lines 52-54). The timeout may be decreased if it is determined to be too long (column 7 line 66- column 8 line 4: the timeout "d" is made "less conservative," meaning it is made shorter). Kwiat discloses that this periodic polling effectively decreases traffic in the system and increases throughput, without creating excessively long delays in fault detection (column 2 lines 33-40, lines 55-62). Olarig wishes to increase the performance of the computer system and minimize failover time (column 2 lines 33-40, 56-62). Using Kwiat's adjustable watchdog timer would decrease the excess load on the memory controller while still maintaining an effective means for fault detection in the memory array. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the adjustable watchdog timer of Kwiat into the memory failover system of Olarig, decreasing the load on the memory controller and maintaining effective fault detection.

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig (United States Patent No. 6,505,305) in view of Nguyen (United States Patent Application Publication No. 2004/0143719), in futher view of Kwiat (United States Patent No. 6,363,496).

As per claim 8, Olarig discloses:

A data processing system, comprising:

a system memory (column 7 lines 32-36);

a memory controller coupled to the system memory and a processor coupled to the memory controller, wherein the controller implements error correction circuitry enabled to identify and correct at least some system memory errors (column 7 lines 43-46);

[a management device coupled to the processor, the management device being enabled to] track the number of errors associated with any particular system memory address (column 10 line 65 – column 11 line 3; column 11 lines 12-16: errors relating to each address are recorded in storage area 328 and the total number of errors for each location is compared to a threshold);

issue a system alert if the number of errors associated with a particular memory address equals a second threshold (column 11 lines 12-16: number of errors compared to a threshold, lines 37-43: an indicator is asserted if the threshold is exceeded)

Olarig does not disclose:

a dedicated interconnect to provide an interrupt signal to the processor wherein assertion of the interrupt signal interrupts the processor (Nguyen ¶ 20: Advance server management line 38);

a management device coupled to the processor, the management device being enabled to;

periodically assert the dedicated interconnect to interrupt the processor and poll system memory error information, including system memory address information, of the processor following each interrupt (Nguyen ¶ 28 lines 1-14);

Nguyen discloses a memory monitoring system which periodically asserts an interrupt to the processor using a dedicated interrupt (Nguyen ¶ 20, ¶ 28 lines 1-14). Nguyen discloses that this enables the system to preemptively examine the memory for errors, instead of waiting for them to occur, enabling the user to be more prepared for undetected memory defects (Nguyen ¶ 5). Olarig discloses that he wishes to prevent situations where catastrophic events cause memory loss and system recoveries (Olarig column 2 lines 32-40). Using Nguyen's system would enable the user to discover a memory is faulty before it actually affects the system, possibly preventing crashes and failed backups from occurring. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the dedicated processor interrupt of Nguyen into the memory failover system of Olarig, preventing crashes and failed backups.

Olarig and Nguyen fail to disclose:

increase the frequency of said polling if the number of errors associated with a particular memory address equals a first threshold; and

Olarig's detects faults by remaining in a constant loop until faults are detected (Olarig column 10 lines 59-67: constant loop at step 400). This requires the memory controller 300 to constantly query the ECC logic component, increasing the activity in the memory controller, and decreasing its ability to perform other tasks, such as controlling data transfer between the processor and the memory array (column 7 lines

32-36: memory controller controls all traffic between processor and memory array). Kwiat discloses a system involving an adjustable watchdog timer which periodically queries a group of components to determine if they are working correctly (column 7 lines 52-54). The timeout may be decreased if it is determined to be too long (column 7 line 66- column 8 line 4: the timeout "d" is made "less conservative," meaning it is made shorter). Kwiat discloses that this periodic polling effectively decreases traffic in the system and increases throughput, without creating excessively long delays in fault detection (column 2 lines 33-40, lines 55-62). Olarig wishes to increase the performance of the computer system and minimize failover time (column 2 lines 33-40, 56-62). Using Kwiat's adjustable watchdog timer would decrease the excess load on the memory controller while still maintaining an effective means for fault detection in the memory array. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the adjustable watchdog timer of Kwiat into the memory failover system of Olarig, decreasing the load on the memory controller and maintaining effective fault detection.

Nguyen also discloses periodic that polling may be performed periodically or in response to faults, (Nguyen ¶ 28 lines 1-14), and that the frequency of faults may increase depending on certain factors (Nguyen ¶ 3 lines 1-6). Nguyen also wishes prevent undetected memory failures from causing a burden (Nguyen ¶ 3). Kwiat's adjustable watchdog timer would frequent interrupts to the processor while still maintaining an effective means for fault detection in the memory array. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to

incorporate the adjustable watchdog timer of Kwiat into the memory failover system of Nguyen, decreasing the load on the processor and maintaining effective fault detection.

As per calim 9, Olarig discloses:

The system of claim 8, wherein the management device is further configured to track the number of consecutive errors associated with any particular system memory address (column 10 line 65 – column 11 line 3; column 11 lines 12-16: errors relating to each address are recorded in storage area 328 and the total number of errors for each location is compared to a threshold);

Olarig does not disclose:

to increase the frequency of said polling if the number of consecutive errors associated with a particular memory address equals a first threshold.

Olarig's detects faults by remaining in a constant loop until faults are detected (Olarig column 10 lines 59-67: constant loop at step 400). This requires the memory controller 300 to constantly query the ECC logic component, increasing the activity in the memory controller, and decreasing its ability to perform other tasks, such as controlling data transfer between the processor and the memory array (column 7 lines 32-36: memory controller controls all traffic between processor and memory array). Kwiat discloses a system involving an adjustable watchdog timer which periodically queries a group of components to determine if they are working correctly (column 7 lines 52-54). The timeout may be decreased if it is determined to be too long (column 7 line 66- column 8 line 4: the timeout "d" is made "less conservative," meaning it is made

shorter). Kwiat discloses that this periodic polling effectively decreases traffic in the system and increases throughput, without creating excessively long delays in fault detection (column 2 lines 33-40, lines 55-62). Olarig wishes to increase the performance of the computer system and minimize failover time (column 2 lines 33-40, 56-62). Using Kwiat's adjustable watchdog timer would decrease the excess load on the memory controller while still maintaining an effective means for fault detection in the memory array. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the adjustable watchdog timer of Kwiat into the memory failover system of Olarig, decreasing the load on the memory controller and maintaining effective fault detection.

As per claim 10, Olarig discloses:

The system of claim 8, wherein the dedicated interconnect is connected to a general purpose I/O pin of the management device.

Nguyen discloses a memory monitoring system which periodically asserts an interrupt to the processor using a dedicated interrupt (Nguyen ¶ 20, ¶ 28 lines 1-14), connected to PCI bus 24 (¶ 19 - ¶ 20, illustrated in figure 1). Nguyen discloses that this enables the system to preemptively examine the memory for errors, instead of waiting for them to occur, enabling the user to be more prepared for undetected memory defects (Nguyen ¶ 5). Olarig discloses that he wishes to prevent situations where catastrophic events cause memory loss and system recoveries (Olarig column 2 lines

32-40). Using Nguyen's system would enable the user to discover a memory is faulty before it actually affects the system, possibly preventing crashes and failed backups from occurring. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the dedicated processor interrupt of Nguyen into the memory failover system of Olarig, preventing crashes and failed backups.

Allowable Subject Matter

Claim 1 was examined and considered allowable over the prior art. The closest available references, Olarig (United States Patent No. 6,505,305) and Kwiat (United States Patent No. 6,363,496), teach similar fault monitoring systems. Olarig's system detects memory faults and alerts a user if too many faults are associated with a given address. Kwiat discloses an adjustable polling system which adjusts the polling frequency in response to faults. However, neither teaches the method of increasing the consecutive fault threshold as well as the polling frequency in response to a fault. This additional step improves the system by adjusting preventing excess alarms due to an increased polling frequency, reducing the burden on the user and the system by preventing any failovers from occurring that are not necessary. Neither Olarig or Kwiat address the situation of increasing polling frequency and its effects on creating excess alarm indications. Therefore, one of ordinary skill in the art would not have been motivated to increase the polling frequency as well as the fault threshold in response to an alert in the memory system.

Claims 2-7 are considered allowable as being dependant on claim 1.

Claims 11-15, 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 11 states:

The system of claim 8, wherein the management device is configured to double the polling frequency and the first threshold value each time the number of errors associated with a particular memory address equals the existing first threshold value.

Claim 12 states:

The system of claim 11, wherein an initial first threshold value is 2 and the second threshold value is 16.

Claim 13 states:

The system of claim 12, wherein the period of the initial polling frequency is approximately 600 seconds.

Claim 14 states:

The system of claim 11, wherein the management device is further configured to reset the polling frequency and first threshold value to their respective initial values periodically.

Claim 15 states:

The system of claim 14, wherein the period associated with resetting the first threshold value is 24 hours.

Claim 20 states:

The management device of claim 16, further configured to increase the first threshold value each time the number of errors associated with any particular memory address equals the first threshold.

Claim 21 states:

The management device of claim 20, further configured to double the frequency of interrupting the processor and the first threshold value each time the number of errors associated with any particular memory address equals the first threshold value.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matt Urick whose telephone number is (571) 272-0805. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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BRYCE P. BONZO
PRIMARY EXAMINER